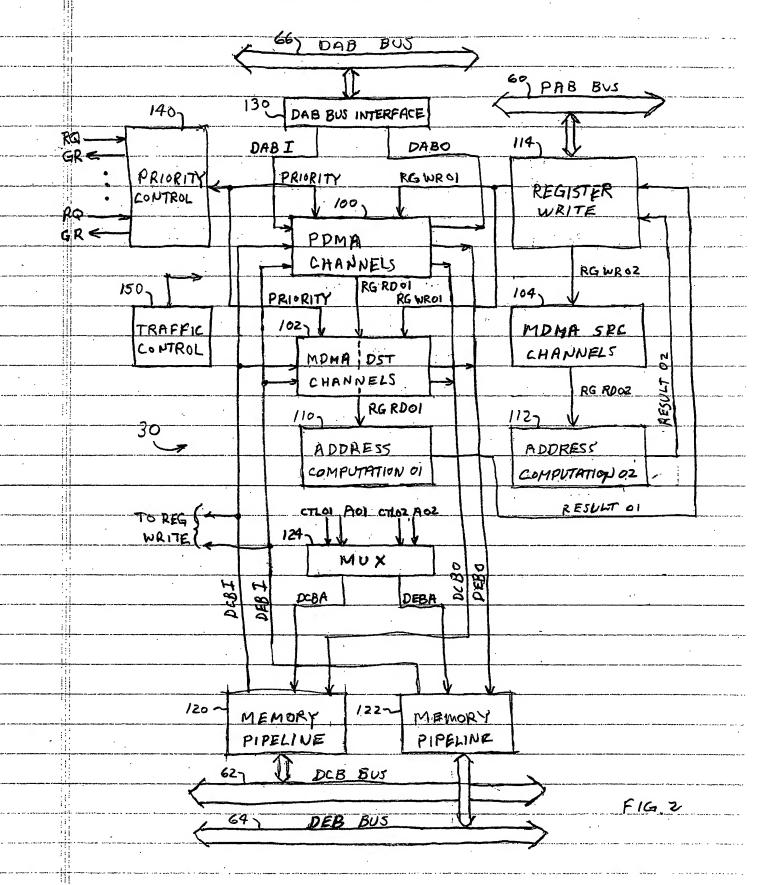
CORF PROCESSOR 16 LI DATA LI INSTRUCTION MEMORY MEMORY 52B 50B 59A 52A BUS INTERFACE 201 62-DCB BUS EAB BUS :11 68-*3*2-30-600 EXTERNAL DMA CONTROLLER PORT DEB BUS 667 DAB BUS 60 PAB BUS PPI 44 SPORT UART SPI

FIG. 1

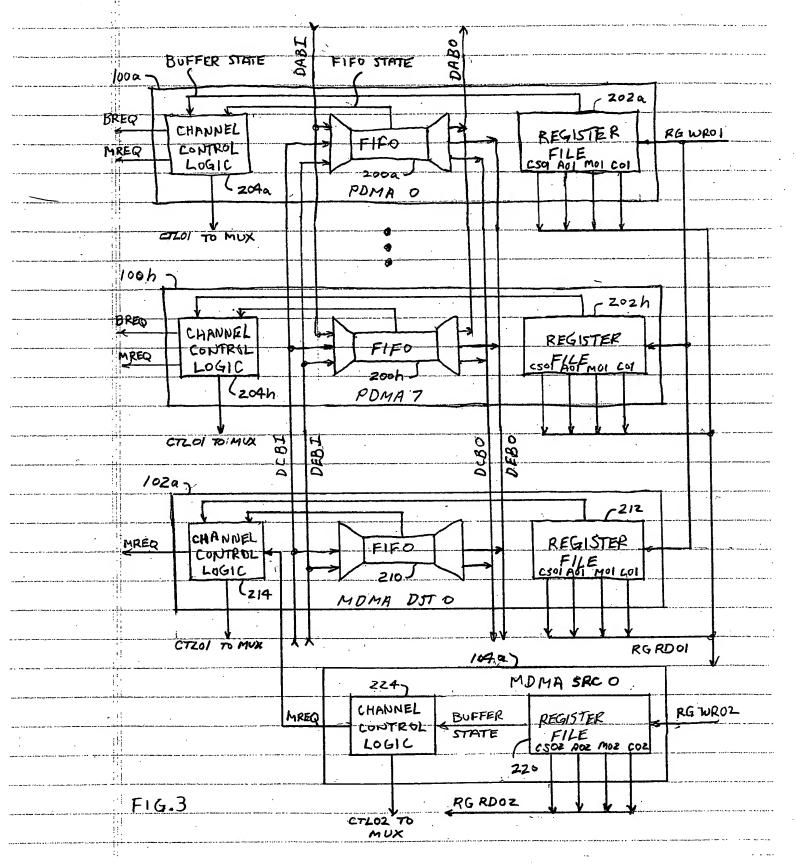
DMA Controller Utilizing Flexible DMA Descriptors John Hayden

Docket No.: A0312.70517US00

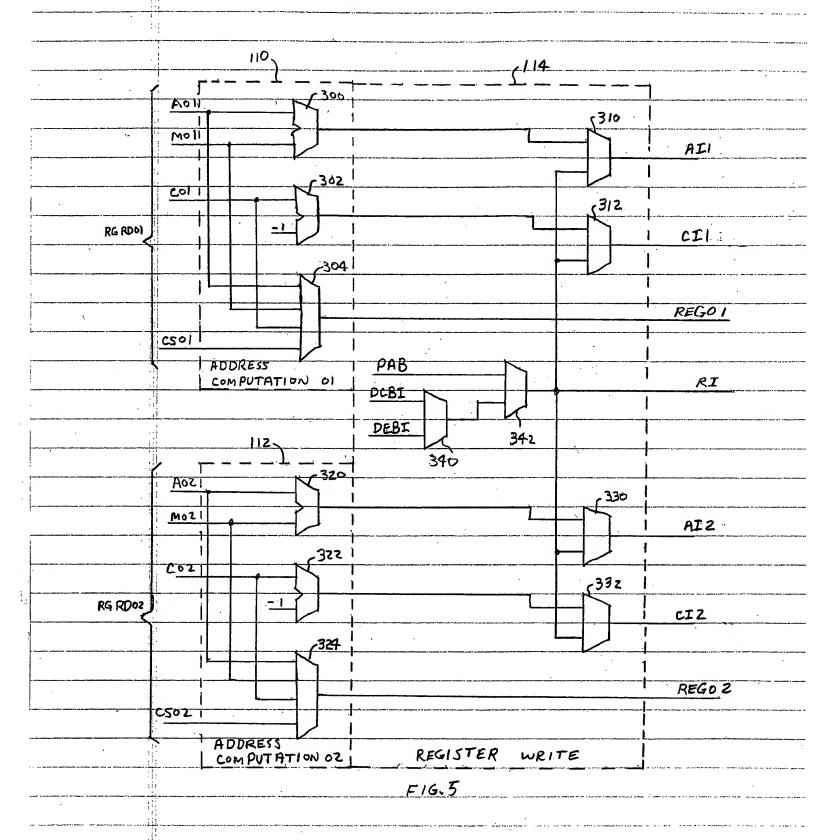


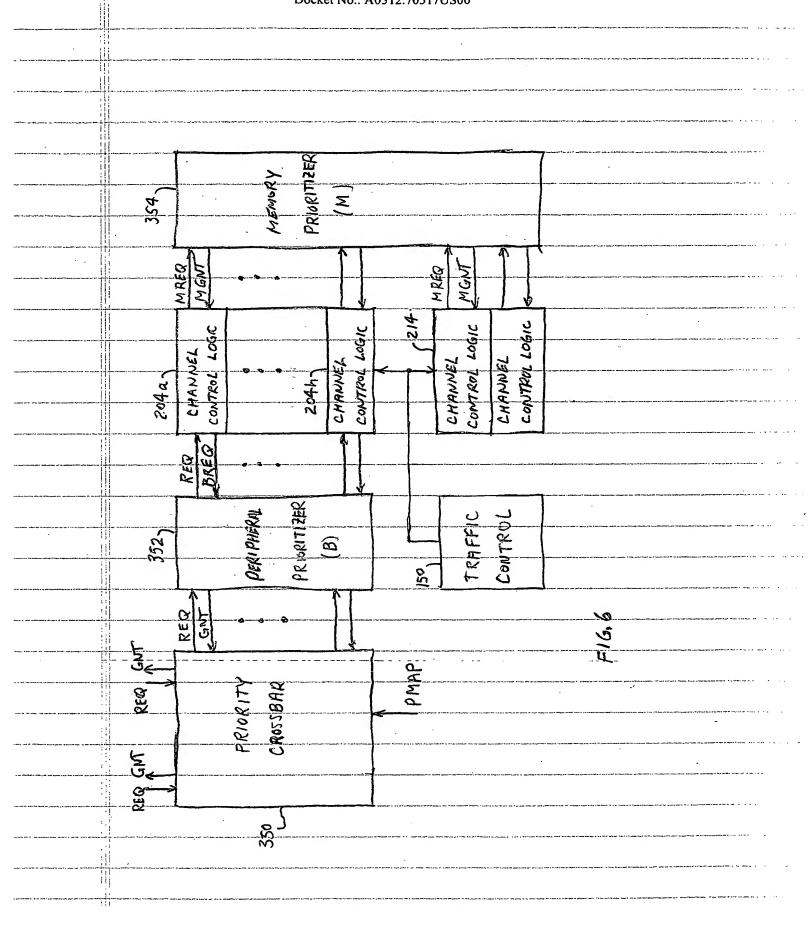
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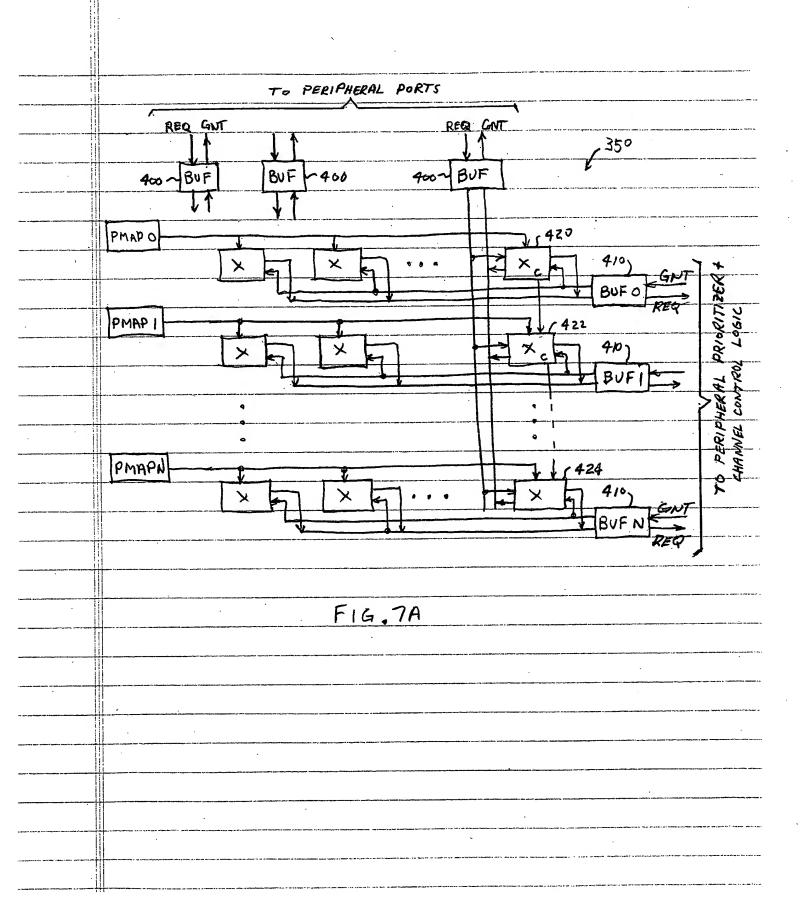
Docket No.: A0312.70517US00

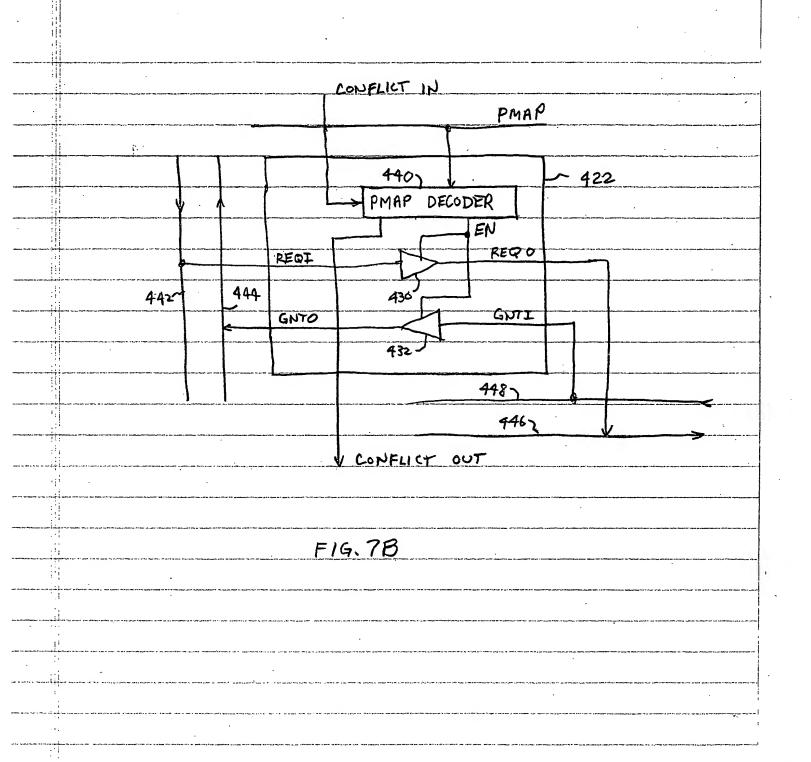


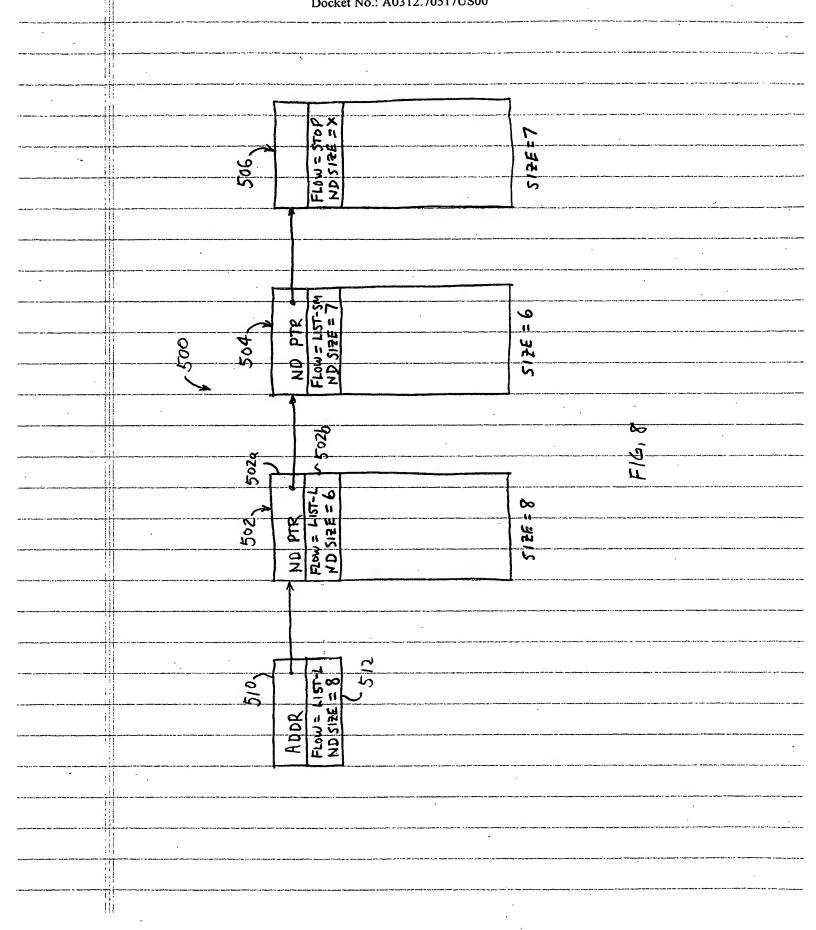
DEBA BUS CONTROL FLOW PIPELINE 75 DEB AACK WRITE DATE DIPELINE ADDRESS + 75 FLOW 5 RACK 5 READ DATA





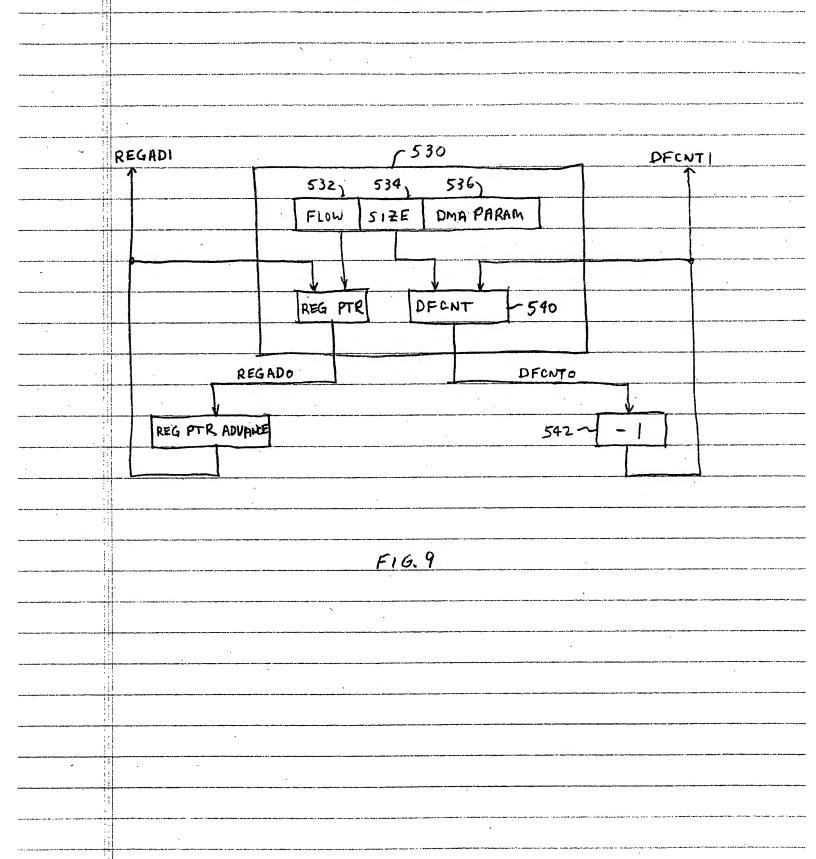


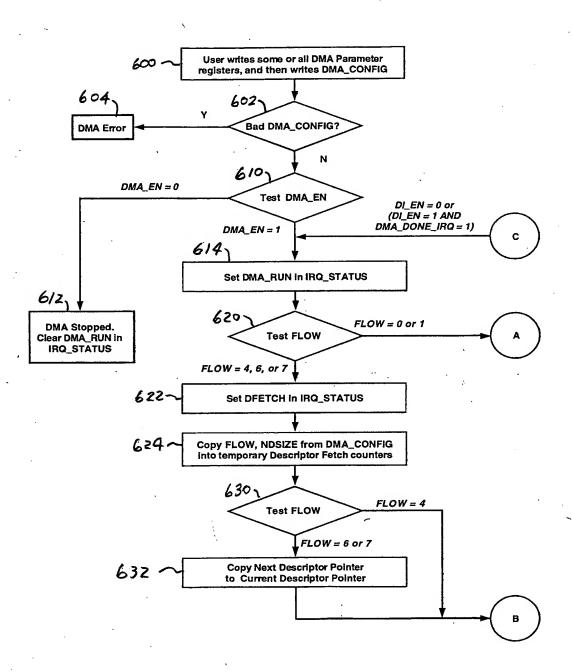




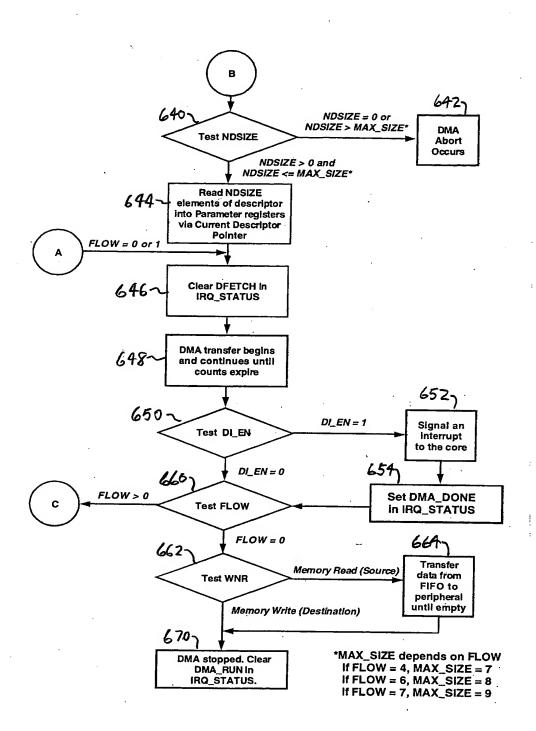
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F16.10



F16.11